POWER AMPLIFIER DESIGN FOR THE 2.11GHZ-2.17GHZ WCDMA BAND USING ADVANCED DESIGN SYSTEM

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Introduction

This application note demonstrates the design of a power amplifier for the 2.11GHz – 2.17 GHz WCDMA band using distributed elements. It features DC simulation, biasing point selection, S-parameter simulation, matching circuit design, optimization, load pull characterization and autolayout. For the purpose of demonstration, the circuit design is kept as simple as possible. Although the GaAs FET FLL101ME from Fujitsu is being chosen for the amplifier, it should be understood that the design procedures demonstrated here are applicable to other GaAs FET.

Theory

High frequency power amplifier is considered as one of the most difficult task in the past. For small signal amplifiers, quasi-linear approximation can be made. Under such approximation, power that can be delivered by the source doesn't have any limit. There is no limit in the current that it can supply and no limit in the voltage that it can sustain across its output terminal.

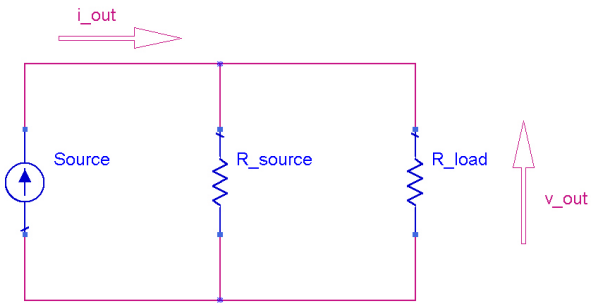

Figure 1. Output Matching of Amplifier

By choosing R_load equal to R_source, conjugate matching is achieved which ensures the amplifier designed gives maximum gain and maximum output power.

But the situation is totally different for power amplifiers. Power amplifiers are operated in large signal region and their behavior is nonlinear. In such region, conjugate match doesn't guarantee maximum output power.

Traditionally, manual or automatic load pull characterization were being employed to search for the optimum impedance for maximum output power. But manual load pull is time

consuming, laborious and unreliable. Automatic load pull system is better, but it is very expensive. Even with automatic load pull system, searching for the optimum output impedance for maximum output power is still time consuming.

With the built-in sophisticated large signal model in ADS, the time consuming and laborious experimental load pull characterization can be avoided. Load pull can be carried out in computer. Multiple design iterations, optimization and tuning can be performed in computer. Thus, the design of power amplifier is more predictable and the design cycle can be shortened.

Setup

1. "FET_Curve_Tracer.dsn" obtains the I-V characteristics of the FET and the biasing point for class AB operation is selected.
2. "Load_Pull_Input_Power.dsn" determines a suitable input power level which can drive the FET into saturation region. The power level determined is used as the input power level in the load pull characterization.
3. "Load_Pull.dsn" determines the optimum output impedance for maximum output power. For simplicity, only the output impedance at fundamental frequency is varied, output impedance at harmonics and input impedance are set as 50Ω.
4. "Output_Impedance_1.dsn" simulates and optimizes the output impedance for maximum output power.
5. "Output_Impedance_2.dsn" simulates and optimizes the output impedance for maximum output power. Damping circuit is added to ensure the amplifier is stable at out-of-band frequencies.
6. "Power_Amplifier.dsn" simulates and optimizes the input impedance for maximum gain.
7. "Power_Amplifier_S.dsn" evaluates S-parameters of the amplifier
8. "Power_Amplifier_PAE_P1dB.dsn" evaluates power added efficiency and output power at 1dB gain compression point of the amplifier.
9. "Power_Amplifier_IMD.dsn" evaluates linearity of the amplifier by two-tone.

Results

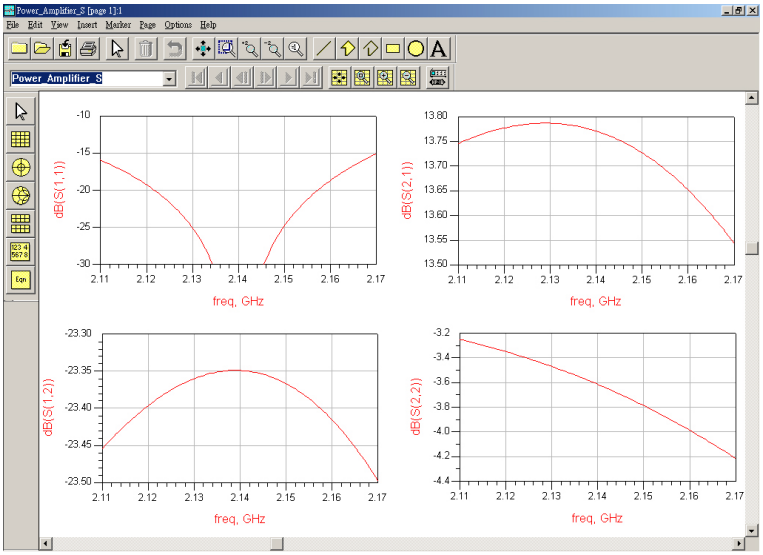

Figure 2. S-parameter of the power amplifier

For the whole WCDMA band, gain of the amplifier is above 13.5dB. The Input return loss, S_{11}, is below -15dB which is considered as good. The output return loss, S_{22}, is around -4dB which is very poor. It is because the output impedance is matched for maximum output power at saturation.

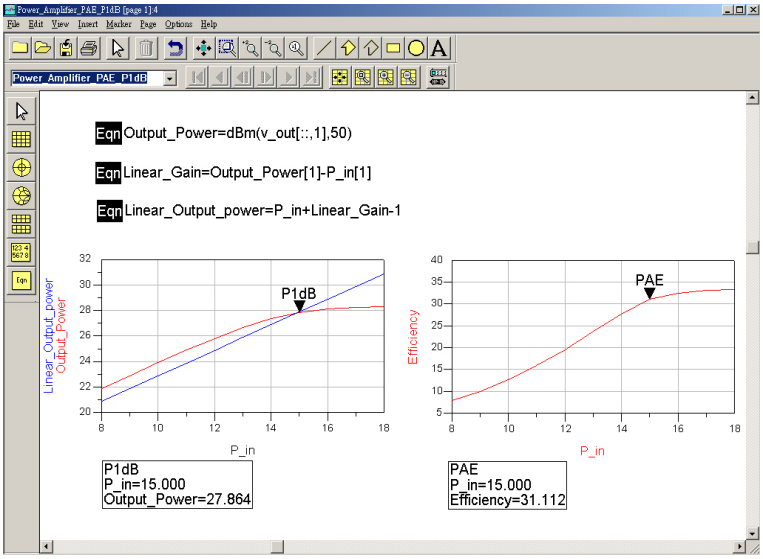

Figure 3. 1dB gain compression point and power added efficiency of the amplifier

1dB gain compression output power of the amplifier is 27.9dBm and power added efficiency is 31%.

Conclusion

In this application note, a power amplifier for the 2.11GHz to 2.17GHz WCDMA band is being designed and simulated. Various simulation techniques have been demonstrated. Gain of the power amplifier is above 13.5dB within the WCDMA band. The amplifier is able to deliver 27.9dBm at 1-dB gain compression point with 31% power added efficiency. It is believed that with Advanced Design System, high frequency power amplifier design can be made easier and more predictable.